CLAIMS

1.   A data communications interface for a node of data processing network, the interface
comprising:

a data transmission path;

a transmission control path;

transmission segmentation logic for receiving a data frame, comprising a transmission
header and a transmission payload, from the node and supplying the transmission payload to
the data transmission path and the transmission header to the transmission control path;

a transmission processor in the transmission control path for controlling
communication of data from the transmission payload to the network via the data
transmission path in dependence on the transmission header;

a data reception path;

a reception control path;

reception segmentation logic for receiving a data packet, comprising a reception
header and a reception payload, from the network and supplying the reception payload to the
data reception path and the reception header to the reception control path; and,

a reception processor in the reception control path for controlling communication of
data from the reception payload to the node via the data reception path in dependence on the
reception header.

2.   An interface as claimed in claim 1, comprising a shared memory and a local bus
providing access to the shared memory by the transmission and reception processors.

3.   An interface as claimed in claim 2 wherein the shared memory comprises a store for
control information to be used by the transmission and reception processors in controlling
said flows of data.

4.   An interface as claimed in claim 2 or claim 3, comprising a communication path for
communicating information between the transmission and reception processors via the shared
memory.

5.   An interface as claimed in any preceding claim, comprising bus interface logic for connecting the local bus, the transmission data channel, and the reception data channel to a bus architecture of the node.

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6.   An application specific integrated circuit, comprising a data communication interface as claimed in any preceding claim.

7.   A network interface card for insertion into a computer system, the network interface

10   card comprising a printed circuit board and a data communications interface as claimed in any of claims 1 to 5 mounted on the printed circuit board.

8.   A computer system comprising: a central processing unit; a memory; a data communications interface as claimed in any of claims 1 to 5; and, a bus architecture

15   interconnecting the central processing unit, the memory, and the data communications interface.

9.   A data processing network comprising a plurality of computer systems as claimed in claim 8 and a network architecture interconnected the computer systems.

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10.   A method of communicating data to and from a node in a data processing network, the method comprising:

      receiving, via transmission segmentation logic, a data frame, comprising a transmission header and a transmission payload, from the node;

25   supplying, via the transmission segmentation logic, the transmission payload to a data transmission path and the transmission header to a transmission control path;

      controlling, via a transmission processor in the transmission control path, communication of data from the transmission payload to the network via the data transmission path in dependence on the transmission header;

30   receiving, via reception segmentation logic, a data packet, comprising a reception header and a reception payload, from the network;

      supplying, via the reception segmentation logic, the reception payload to a data reception path and the reception header to a reception control path; and,

controlling, via a reception processor in the reception control path, communication of data from the reception payload to the node via the data reception path in dependence on the reception header.